

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: **FABRICATING STRAINED CHANNEL
EPITAXIAL SOURCE/DRAIN TRANSISTORS**

INVENTORS: **Anand Murthy, Justin K. Brask,
Andrew N. Westmeyer, Boyan Boyanov,
and Nick Lindert**

Express Mail No. EL 990 136 159 US

Date: February 17, 2004

FABRICATING STRAINED CHANNEL
EPITAXIAL SOURCE/DRAIN TRANSISTORS

Background

This invention relates generally to the fabrication of integrated circuits.

Transistors utilized in logic circuits have a current
5 drive that is proportional to the mobility of charge carriers. Current drive is related to speed. Thus, it is desirable to improve the mobility of charge carriers.

It is known to use strained channel epitaxial source/drain transistors for the p-channel transistors.
10 The source and drain are formed by ion implantation. The implanted source/drain is then removed using an etching process. A germanium doped silicon material is then selectively deposited into the source/drain regions.

Because germanium expands as it becomes epitaxial, it
15 compresses the channel between source and drain, increasing the mobility of the charge carriers through the channel. However, the need for selective deposition of the epitaxial source/drain raises yield concerns.

Thus, it would be desirable to have alternate ways to
20 form strained channel epitaxial source/drain transistors.

Brief Description of the Drawings

Figure 1 is a greatly enlarged, cross-sectional view at an early stage of manufacture in accordance with one embodiment of the present invention;

5 Figure 2 is a greatly enlarged, cross-sectional view corresponding to Figure 1 at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

10 Figure 3 is a greatly enlarged, cross-sectional view corresponding to Figure 2 at a subsequent stage of manufacture in accordance with one embodiment of the present invention; and

15 Figure 4 is a greatly enlarged, cross-sectional view corresponding to Figure 3 at a subsequent stage of manufacture in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a pair of transistors 10a and 10b may be formed in a semiconductor substrate 12. The
20 transistors 10a and 10b may both be PMOS or one may be NMOS and one may be PMOS. Initially, source/drains 20a and 20b are formed in the substrate 12 using a gate electrode structure as a mask. The gate electrode structure may include a gate electrode 14 and sidewall spacers 16. An
25 isolation trench 18 may electrically isolate the transistor 10a from the transistor 10b.

Referring next to Figure 2, the implanted source/drains 20a and 20b may then be removed using a well known dry etch, leaving depressions 22 at the locations where the source/drains previously existed.

5 Referring to Figure 3, in the case of an NMOS transistor, carbon doped silicon film 24 may be blanket deposited over the active area of the transistor 10a. The blanket deposition may be a chemical vapor deposition using trisilane, methyl silane, and H₂ at a deposition temperature
10 less than 550°C in one embodiment. At these temperatures, the film 24 is rendered epitaxial on the exposed silicon regions 22 and is amorphous on oxide and nitride areas such as the sidewall spacer 16. The carbon doped silicon film 24 may also be *in situ* doped with phosphorous or arsenic
15 during deposition in one embodiment.

In a single wafer 300 millimeter rapid thermal chemical vapor deposition (RTCVD) reactor, a chemistry of 20 sccm of trisilane, 30 sccm of mono-methyl silane, 20 slm of H₂, at 550°C, and 15 Torr pressure for 12 minutes
20 produces a 50 nanometer carbon doped silicon film 24 with a fully substituted carbon concentration of 3E20 cm⁻³.

An amorphous layer 26 is formed in regions not in contact with the silicon substrate 12. Thus, the amorphous layer 26 covers the gate electrode 14 and sidewall spacer
25 16. One reason for the formation of crystalline material 24 in the substrate 12 is that, in the substrate, the

silicon continues to grow epitaxially expanding the existing lattice. However, there is no existing lattice to support growth of the crystalline film over areas outside the silicon substrate 12.

5 In the case of the PMOS transistors, a boron doped silicon germanide film may be deposited non-selectively after etching out the implanted sources and drains. An amorphous film 26 forms over oxide and nitride areas while a crystalline film 24 forms within the substrate 12.

10 Then, as shown in Figure 4, in both the NMOS and PMOS examples, the amorphous film 26 is selectively etched away without adverse consequences to the epitaxial source/drain film 24. Selectivity to amorphous silicon over crystalline silicon may be achieved by tailoring the etch chemistry
15 utilizing differences in the activation energy towards forming the dissolution products. Where a film crystallizes a lot of energy is gained. The etch may be tuned so it does not overcome the activation barrier needed to etch material in the crystalline phase.

20 Highly carbon doped crystalline silicon provides the barrier to remove the dissolution products due to non-degeneracy in the lattice. Amorphous film (doped or undoped) has insufficient lattice energy to overcome the activation barrier.

25 A chemistry comprising 15% NH_4OH in deionized water with sonication is effective in removing the amorphous

silicon without etching the doped crystalline silicon. As another example, 25% tetramethylammonium (TMAH) in deionized water also with sonication may be used.

In one embodiment, the sonication may involve the application of sonic energy in the frequency range between approximately 10 kilohertz (kHz) and 100 kilohertz. In a second embodiment, the sonication may be megasonic, namely the application of sonic energy in the frequency range between approximately 500 and 1000 kilohertz. The etching may be performed in a wet etch bath. The wet etch may be performed by immersing a wafer in an etchant. For example, the wafer or wafers may be immersed in a tank, such as a chemical bath, that is equipped with sonication. The equipment for sonication may vary, but in one embodiment using ultrasonic or megasonic frequencies, transducers located external to the tank may provide sonic waves at the desired frequency.

Once the amorphous silicon 26 has been removed, the highly carbon doped silicon film 24 is retained in the N⁺ source/drain regions. Likewise, the boron doped silicon film 24 may be retained in P⁺ source/drain regions. The remaining fabrication may use standard CMOS fabrication steps, including source/drain lithography, source/drain implants, rapid thermal anneals, and salicide formations, in one embodiment.

As a result, high tensile strain can be generated in the NMOS transistor channel and high compressive strain may be generated in the PMOS transistor channel, thereby realizing mobility and performance gains. Because of the non-selective epitaxial deposition, simplicity and flexibility may be achieved in some embodiments. Yield risks associated with selective deposition may be reduced in some applications.

In the case of the NMOS transistors, a relatively high concentration of carbon may be obtained during the blanket or non-selective deposition. The higher substitutional carbon results in greater channel mobility.

In addition, chlorine containing silicon precursors are not needed in some embodiments of the present invention. Avoiding the need for chlorine containing silicon precursors increases the deposition rate in some embodiments.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: